Optically Addressed Ferroelectric Memory With Non-Destructive Read-Out

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ABSTRACT

This paper will present a review of the emerging "Optically addressed ferroelectric memory with non-destructive read-out (NDRO)" as a non-volatile memory technology, identifies its high impact applications, and identifies the necessary conditions for its realization. Based on the high speed, bidirectional, polarization-dependent photoresponse, simulation of a readout circuit for a 16 K VLSI ferro-memory chip yields read access times of ~ 20 ns and read cycle times of ~ 30 ns, (~ 35 ns and ~ 45 ns, respectively, within a framework of radiation-hard environment) , easily surpassing those of the conventional electrical destructive readout. Extention of the simulation for a 64K memory shows that the read access and cycle times are only marginally increased to ~21 ns and ~31 ns, respectively (~38 ns and ~ 48 ns, with a radiation-hard readout circuitry). In addition, the optical NDRO signal offers itself as a unique tool that allows a non-destructive 'probe' for the capacitor, without causing any polarization switching in it, the characteristic artifact of the electrical destructive readout measurement technique. Commercial realization of the optical NDRO, however, would require a reduction in the incident (optical) power by about an order of magnitude for the readout; and an enhancement in the delivered power\size ratio of semiconductor lasers for compact. implementation. A novel device design based on PZT with the c-axis parallel to the substrate is suggested to reduce the requirement of incident optical power further down by orders of magnitude with potential to realize such a memory. This paper presents a new two-capacitor memory cell configuration that provides an enhanced bipolar optoelectronic response from the edges of the capacitor at incident optical power as, low as ~ $mW/\mu m^2$. In addition to the potential of such photoresponse as an NDRO signal, its dependence on the "product" of memory stored and incident optical signal offers opportunities for high speed analog optoelectronic computing, optical communication networks, image processing, and highly parallel processing architectures such as optoelectronic neural networks for on-board processing.

I Introduction

Ferroelectric memories are of considerable interest for applications such as optical information storage or correlation[1-4]. However, it is well recognized that only non-destructive read-out (NDRO) of ferroelectric nonvolatile memories would truly exploit the full potential of such ferroelectric optical memories[5-9]. An electrical NDRO method utilizes a ferroelectric field effect transistor configuration where modulation of the source-to-drain current across a semiconductor channel is accomplished by the remanent polarization (memory) in a ferroelectric layer in the gate region. Although nondestructive to the memory, this scheme[10] involves the challenge of optimizing a ferro-semiconductor interface. In implementations to-date[9-11], the fast ferroelectric polarization switching is generally accompanied by undesirable effects such as the slowly drifting injected space charge at the ferroelectric/semiconductor interface contributing to deleterious modulating fields. Also, retention loss due to leakage associated with the semiconductor/ferroelectric interface is a problem. Efforts[9,12] are underway to replace lead zirconate titanate by barium magnesium fluoride, $BaMgF_4$ and/or bismuth titanate, $Bi_4Ti_3O_{12}$ in search of a better ferroelectric/semiconductor interface. The retention time however has been limited to a matter of hours in these cases.

On the other hand, the concept of the optically addressable NDRO could truly exploit the demonstrated retention time of over

several years [13-15] of lead zirconate titanate (PZT) capacitor based memories. This concept of optical NDRO is based on the polarization dependent photoresponse from a ferroelectric capacitor; without substantially changing its physical configuration or subjecting it to the stringent requirement of a semiconductor/ferroelectric interface. When the wavelength of the incident radiation is less energetic than the bandgap of the PZT material, the stored memory state is not altered by the incident photons. This non-destructive feature can make the ferroelectric memories an excellant candidate for critical data storage. In addition, such a non-destructive readout (NDRO) may also offer the ferroelectric nonvolatile memory for analog applications. The constant memory refresh required in the conventional destructive readout (DRO) does not sustain the bit level precision required for an analog memory operation. Furthermore, such a memory-modulated analog photoresponse available from a monolithic "programmable detector" may find applications in the backplane of optical computers as a compact, smart detector array, potentially replacing a combination of spatial light modulators and detectors. This potential emerges from the dependence of the photoresponse on the analog "product" of the memory stored and 'the incident optical signal. Such functionality from an integrated, 'compact device, with simpler fabrication and enhanced speed by parallel access, offers opportunities in a wide spectrum of applications including high speed analog optoelectronic computing, optical communication networks, image processing, and parallel processing architectures

such as optoelectronic neural networks.

We have previously reported[7,16] on a high speed, bidirectional, polarization dependent photoresponse from ferroelectric thin film capacitors, as a high speed optically addressed (λ= 532 nm) NDRO[17] of the non-volatile memory (remanent polarization). This paper presents a critical assessment of its potential as a memory technology and conditions for realization of this technology for its high impact applications.

II Experimental Details

In order to determine the technological viability of the optically addressable memory with NDRO, we have initially focussed on the conventional Pt/PZT/Pt - sandwich device configuration A (figure 1a), with a nominal goal of a 16 K memory chip design.

1. Computerized MultiProbe Test Assembly:

A computerized multiprobe test setup including a compact laser has been assembled, to allow a study of the high speed photoresponse and a comparison of the optical NDRO results with the conventional DRO technique, which has been described in detail elsewhere[18,19]. This set-up allows measurement and recording of optical NDRO behavior of the ferroelectric capacitor, along with conventional electrical DRO signal (pulse measurement using virtual ground

circuit) , Sawyer/Tower hysteresis loop, capacitance, and resistance /leakage, etc; on the same sample without disturbing the probes. This highly integrated setup is quite flexible, versatile, interactive, and allows convenient computer storage and analysis of the data. In particular, the flexibility of subjecting a sample to the various probes, repeatedly, in any selected sequence, with a verifiable guarantee that the sample has not been irreversibly altered during the course, is extremely valuable in correlating the various phenomena studied. The small (30 cm long) laser, with a variable attenuator for controlling the incident power, has FWHM of 6 ns. The sample stage was capable of XYZ motion as well as the focussed illumination beam could be moved independently in the XY dimensions to record the photoresponse with different illumination profiles for the same illumination power on different configurations of the device.

2. Device Fabrication and Photoresponse Investigation:

A variety of device test structures in the sandwich configuration were fabricated using c-axis oriented PZT thin films with either platinum or conducting lanthanum strontium cobalt oxide (LSCO) as the top electrode. The thickness of the top electrode ranged from a semitransparent 100 A layer to a 3000 A thick opaque reflective layer. The diameters of the capacitors ranged from 100 μm to 250 pm. Comparison of the photoresponse results from the semitransparent and opaque top electrodes suggested that at power

levels ≥ 20 mW/μ^2, the hi-directional polarization dependent photoresponse is due to a thermally triggered mechanism. In the following, we present a memory design based on this response, estimated power requirement for it, and projected performance levels for the basic sandwich device (configuration A, figure la) as well as for a device structure (configuration B, figure lb) with a modified top electrode, which would enhance its optical absorption characteristics.

In addition, our recent results[16] on the optoelectronic effects at an order of magnitude lower power levels (' 2 mW/μ^2) from the edges of the PZT capacitor have led to a two ferro-capacitor memory cell with significantly enhanced readout. High speed bipolar optical NDRO results from such two capacitor combinations are discussed leading to the suggestion for a novel device design (configuration C, Figure lc).

III. VLSI IMPEMENTABILITY

A. A Baseline Memory Cell Design (configuration A) :

As a baseline, the photoresponse at a wavelength of 532 nm at 20 mW/μ^2 incident optical power[7] was utilized with a single ferrocapacitor memory cell. This design is preferred over the two capacitor differential signal sensing design for smaller cell size as well as faster access. The bidirectional nature of the response allows the flexibility of utilizing a single ferrocapacitor cell.

We have adapted a typical DRAM circuit design without refresh that utilizes standard balanced bit line technique for the bit differentiation based on the photoresponse input signal. A block diagram and schematic of the configuration is shown in Figure 2a. Fig 2b is a circuit diagram of the typical column read functional cell. SPICE simulation programs were developed for estimation of the performance parameters of the sensing circuit. The calculations and speed figures are based on the simulated. and measured data for existing RAM designs using a two balanced lines per bit design. The analysis is divided into three categories: (1) Ferroelectric cell model, (2) Support circuitry timing and (3) Support circuitry area.

Ferroelectric Cell Model:

Utilizing a typical photoresponse data[7,8], we have modeled the ferroelectric capacitor as a current generator with estimated constants of capacitance C_f 0.4 $pf/\mu m^2$ and current I_f 0.32 $\mu A/\mu m^2$. In order to perform area calculations and to determine initial bit line capacitance, it was necessary to produce a prototype layout of the cell. A conservative assumption was made that the ferroelectric cell could be placed within 2 minimum dimensions of other structures in a 1.2 μ CMOS process. Furthermore, it was assumed that the ferro-capacitor is constructed of two overlapping layers, each immediately contactable from metal one. Also it is assumed that the illumination rise times and

durations are available that lead to current waveforms with rise times on the order of 1 ns or slower and durations on the order of 10 to 100 ns.

Support Circuitry Timing :

The support circuitry timing must account for the following delays:

(1) Bit-line delay (T_b): The time for voltage on the bit line to reach a nominal value v_b. v_b is the minimum differential voltage required to activate the comparator and is chosen with consideration for the noise environment, the typical offsets of the bit line comparators, and the minimum expected current capability of the ferroelectric capacitor.

(2) Comparator delay (T_c): Time taken by the comparator to make a decision.

(3) Other peripheral electronic timing delays (T_e) include the addressing, multiplexing and setup delays. Addressing delay is the time to drive the address lines and enable one ferro-capacitor onto each column. Multiplexing delay is the additional delay to multiplex the requested column/bit into one bit and the setup time to register the output is considered as the setup delay.

The total access time is a summation of all these three individual time delays.

$$T_{access} = T_b + T_c + T_e$$

Further, to obtain the read cycle time, T_{cycle}, the additional time to re-balance, or precharge ($T_{precharge}$) the bit lines is then added to the above evaluated read access time.

Support Circuitry Area:

The area of the ferrocell support circuitry, mainly the address enable MOSFET, is used to allow calculation of the area of the core for various memory configurations. An assumption was made that unconstrained area and drive capability is available outside the periphery of the core itself. None of the requirements for drive or timing are difficult to achieve in a standard 1.2μm process, and in fact, the requirements imposed by the ferrocell design used here are quite similar to conventional DRAM.

The results of the circuit simulation are presented in Table I. In addition to the results for a 16K chip, the table also shows simulation results for a 64K chip. Clearly, a scale-up from 16K to 64K chip does not unduely impact the read access time, increasing only slightly from 19.58 ns to 21.33 ns. Further increase in memory density or size (say, 256K and beyond) will however have to depend on both, advanced readout circuitry to maintain the high 1/0 speed, as well as optimization of the materials/device configurations for enhanced photoresponse. For example, the novel device configuration based on PZT with the c-axis parallel to the substrate suggested in the following would make full use of the

potential of optoelectronic effect to achieve higher memory density.

B. Radiation Considerations for Ferroelectric Memory Readout Electronics:

The simulation framework utilized here is based on generic design parameters from a commercial CMOS VLSI process, available through Metal Oxide Semiconductor Implementation Service (MOSIS). This process is typically good for ~ 20 KRads before serious degradation occurs. With nominal operation conditions, a read access time of < 20ns could be obtained using such a process with minimum feature size of 1.2 μm. Lowering the feature size to 0.8 μm will further improve the speed. Using data[20] obtained from experiments conducted on the Combined Release and Radiation Effects Satellite (CRRES), a 20-30 KRad total dose impingement is projected to result in a speed degradation by a factor of about 2. This degradation is applicable to times T_c and T_e. Using this modification, simulation for a 16K chip yields an increase in access time from 19.58 ns to 34.25 ns, that allows for a margin for radiation hardness. For further ruggedness of the device, one could use a dedicated radiation hard (> 1 MRad) fabrication process.

c* Architecture for Compact Implementability :

Figure 3 shows the memory architecture proposed for a dual

ferroelectric-laser chip pack where a laser chip would be flip-bonded on top of the ferro-chip. Feasibility of such a chip design in a compact manner however would rely on bringing, the optical power requirement down to about 0.1 $mW/\mu m^2$, so that demonstrated[21] laser technologies (VCSEL technology with individual row addressability) may be utilized (with '1 W of wall plug power requirement) to build such an optically addressable chip. At the cost of more real estate and a'n order of magnitude more wall plug power, the chip pack may be implemented with today's state-of-the-art lasers. Figure 4 shows a conceptual design of the chip with monolithically integrated strips of edge emitting lasers, modified further for surface emission with 45" etched mirrors or diffraction grating. With the present requirement of about $2mW/\mu m^2$ of peak power, assuming readout of one word or one row/column at a time from a 16K architecture, a wall plug power of about 15 W will be required for such an arrangement. On the other hand, when the desired goal of '0.1 $mW/\mu m^2$ of sensitivity is achieved, the wall plug power demand would drop to about a Watt, making it comparable to the other non-volatile memory technologies (e.g. EEPROMS or electrically read ferroelectric memories).

IV. Novel device configuration based on photoresponse from the Edges:

We have recently reported[16] on a novel optoelectronic response observed essentially from the edges of the thin film ferroelectric

capacitor as confirmed by moving around the beam spot across the top electrode. This photoresponse from the edges occurs at power level which is an order of magnitude lower ‘than that for the thermally triggered response[7]. The PZT in these capacitors has a preferential c-axis orientation perpendicular to the substrate. With an assumption that the photoresponse is a direct consequence of aligning the E - field of the incident optical beam with the c - axis of PZT, the area under the electrode with c axis perpendicular to the optical E field may not even contribute to the response. Instead, domains that may actually contribute to the photoresponse may be from the smaller population of non-c-axis oriented domains from the edge regions (tilted, and therefore, aligned at least in part with the optical E field during readout, and initially aligned in part with the polarizing field direction during 'writing'. The observation of the response preferentially from the edges therefore suggests that the response is a strong function of the crystalline orientation of the film.

The new device configuration introduced herein is a combination of two capacitors that exhibits a bipolar response, based on the optoelectronic effect obtained preferentially from the edges[16]. Figure 5 shows the new device configuration consisting of two capacitors, connected back-to-back by the base electrode, and the corresponding net photoresponses obtained from it when the optical beam is made incident on it at’ different places, as shown in the figure. For the reference of the photoresponse polarity, the top electrode of the left capacitor (Al) is grounded. Figures

5(a) and 5(c) show the responses essentially from the left (Al) and right (A2) capacitors, respectively, when illuminated individually. Whereas, figure 5(b) shows the net bipolar photoresponse from the capacitor-pair (illuminated as shown in the figure), which directly reflects the direction of the remanent polarization in the capacitors. The "spacing" between the two capacitors in this twin cell experiment ranged from 100 to 500 microns. Figure 6 shows typical photoresponse outputs from such a twin cell experiment where 6(a) is the background/noise signal (recorded with the device in the dark) due to the pick up of the Q switching high voltage of the Nd-YAG laser by the sample electrodes (which act as antenna), and Fig 6(b) and 6(c) are the responses for the positively poled and negatively poled sample combinations respectively. Further, figure 6(d) and 6(e) are the difference signals between the illuminated response for the positively poled state and the negatively poled state and the dark noise signal respectively. A retention study[22] of remanent polarization in a ferroelectric capacitor utilizing the conventional DRO illustrates the variability of non-switched charge in the DRO measurement as a major problem for apparent retention loss, and speculates on possible mechanisms for the loss. Clearly, the optical NDRO provides a unique non-destructive probe[16,18,23,24] for ferroelectric capacitors without causing any additional polarization switching, an artifact of the conventional DRO.

Finally, based on observation of this bipolar response from a

two capacitor combination, we have conceptualized a device structure shown in Figure lc. This new device design consists of a planar geometry where PZT would have its c axis parallel to the substrate plane, and the two metal electrodes for write as well as read operations would be laterally separated as shown. This would utilize the polarization dependent photoresponse (such as shown in figure 6d and 6e), already at lower optical incident power ($\sim$2 $mW/\mu m^2$) by an order of magnitude, as a bidirectional measure of the polarization state of the memory. Using a suitable template layer such as MgO and selection of the growth conditions (substrate temperature and ambient partial pressure) polycrystalline/epitaxial films with c axis parallel to the substrate could be deposited as has been demonstrated in the case of YBCO[25], $BaTiO_3$ [26], $PbTiO_3$ 27 and lead zirconate titanate[28]. The proposed device with the planar geometry would allow ease of polarization of PZT in the planar (c-axis) direction with two distinct polarity options. Moreover, the incident light beam would illuminate (and therefore address) the full area of active, polarized PZT for substantially increased signal. This configuration is similar to the one studied by Bass and others[29-31] in a variety of ferroelectric single crystals to observe the optical rectification effect. Also, it is noteworthy that this configuration is a single cell device that exploits the bipolar nature of the response.

v. Power requirements study:

The power requirement for the three device configurations is addressed individually in the following:

Device Configuration A (figure 1a) refers to the conventional Pt/PZT/Pt sandwich structure. The circuit simulation results summarized in table 1 project a read access time ~ 20 ns and read cycle time ' 30 ns for a 16K chip fabricated using a commercial VLSI fabrication process with no rad-hard margins. Including the rad hard margins the read access time is ~ 35 ns and read cycle time is " 45 ns. Although the access speed projected above is competitive and offers an edge over other nonvolatile memory technologies, such a device would require ~ 20 $mW/\mu m^2$ of power for the optical NDRO. Compact semiconductor lasers in that power range are not available at present. Commercial semiconductor lasers currently available can deliver only ' 0.01 $mW/\mu m^2$ and devices demonstrated in the laboratory deliver[21] ~ 0.1 $mW/\mu m^2$ at this time.

Alternatively, diode laser pumped solid state lasers along with an acousto-optical scanning system may be packaged in a size of ~ (10 x 6 x 6) cm^3 box along with an electronic circuitry of the size of a cube of 10 cm on each side. However, the scan rate would limit the read frequency to about a Megahertz, and the wall plug power requirement for such a package would exceed 10 watts.

Device Configuration B (figure lb) is essentially the same sandwich device described above except for replacement of the highly reflective platinum top electrode (optical absorptivity '1%) by a better absorptive layer (e.g. a Platinum cermet film with an absorptivity in excess of '80%) It would clearly reduce the required peak power per pixel to below " 0.5 $mW/\mu m^2$, however even that needs to await about a five fold enhancement in the power to size ratio in order to allow a compact implementation (figure 5) as a dual chip with a flip bonded semiconductor laser chip onto the ferroelectric chip.

Also, in this thermally triggered read mechanism the read access cycle time for the same bit would be as long as a fraction of a microsecond, due to the extended oppositely directed relaxation observed[7] in the photoresponse.

Device Configuration C (figure 1c) is the proposed device with the planar geometry which would allow ease of polarization of PZT in the planar (c-axis) direction with two distinct polarity options. Moreover, the incident light beam would illuminate (and therefore address) the full area of active, polarized PZT for a substantially enhanced signal. Further, the new configuration will allow an optimum[30] 900 incidence of the optical beam thus giving another factor of 20% to 30% over the currently measured value. Consistent with the single crystal results[31], the extent and direction of rectification is found to vary with the polarization of the

incident beam and the angle of incidence. Therefore the choice of the angle of incidence and the illumination polarization[32] do allow one to obtain maximum contrast between the photoresponses from the two states of the poled capacitor.

Overall, therefore one expects a substantial (orders-of-magnitude) enhancement in photoresponse from this new configuration leading to the desired operational power/size ratio of about 0.01 mW/μ^2, readily implementable with the current semiconductor laser technology. However, exact quantitative estimate of the response signal will have to await a detailed" device modelling and simulation.

VI. Summary:

1. Based on the high speed, bidirectional, polarization-dependent photoresponse, simulation of a readout circuit for a 16 K VLSI ferro-memory chip yields read access times of ~20 ns and read cycle times of ~30 ns, (~ 35 ns and " 45 ns, respectively, within a framework of radiation-hard environment), easily surpassing those of the conventional electrical destructive readout. Extention of the simulation for a 64K memory shows, that the read access and cycle times are only marginally increased to '21 ns and "31 ns, respectively ("38 ns and ~48 ns, with a radiation-hard readout circuitry) . Commercial realization of the optical NDRO, however, would require either a reduction, by about an order of magnitude, in the incident

(optical) power for the readout; or an enhancement by about an order of magnitude in the delivered power/size ratio and reduction in production cost of the semiconductor lasers to be used for the optical addressing.

2. A high speed (~10 ns) bidirectional, polarization-dependent photoresponse is observed from a twin ferro-capacitor test structure illuminated with ~$mW/\mu m^2$ of incident optical power.
3. A conceptual device design based on PZT films with c-axis parallel to the substrate is presented. With its substantially enhanced photoresponse, It would potentially reduce the requirement of incident optical power for high speed NDRO by orders of magnitude thus leading to commercial realization of this technology.

Further, the optical NDRO may also provide a unique non-destructive probe for ferroelectric capacitors without causing any additional polarization switching, an artifact of the conventional DRO.

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Figure Captions:

Figure l(a): Schematic cross-section of device configuration A

Figure l(b): Schematic cross-section of modified device configuration B to maximize thermally triggered NDRO response.

Figure l(c): Schematic cross-section of the new device configuration C that maximizes the newly observed optoelectronic NDRO response.

Figure 2a: Block diagram of the memory chip configuration.

Figure 2b: Circuit diagram of a typical column read functional cell.

Figure 3: Illustration of an optically addressable ferroelectric memory - semiconductor laser dual chip pack.

Figure 4: Layout of a 16K optically addressable ferroelectric chip utilizing bars of edge emitting lasers made surface emitting by etching mirrors or diffraction grating.

Figure 5: Summary of the optoelectronic effect observed' from a combination of two ferroelectric capacitors, the illumination profiles used and the respective photoresponses obtained.

Figure 6a: NDRO photoresponse signal from a ferroelectric test structure in the dark (noise signal) consisting of combination of two ferroelectric capacitors with central illumination as illustrated schematically in figure 5 (b).

Figure 6b and 6c are photoresponses (measured as voltage drop across a 50 Ω impedence) in response to the 6 ns laser pulse at 532 nm wavelength for the positively poled and negatively poled state of the 'two ferro-capacitor' memory cell respectively.

Figure 6d and 6e: Net photoresponse obtained as a difference of pulse illuminated signal and dark signal for the positively (6b-6a) and negatively poled state (6c-6a) respectively.

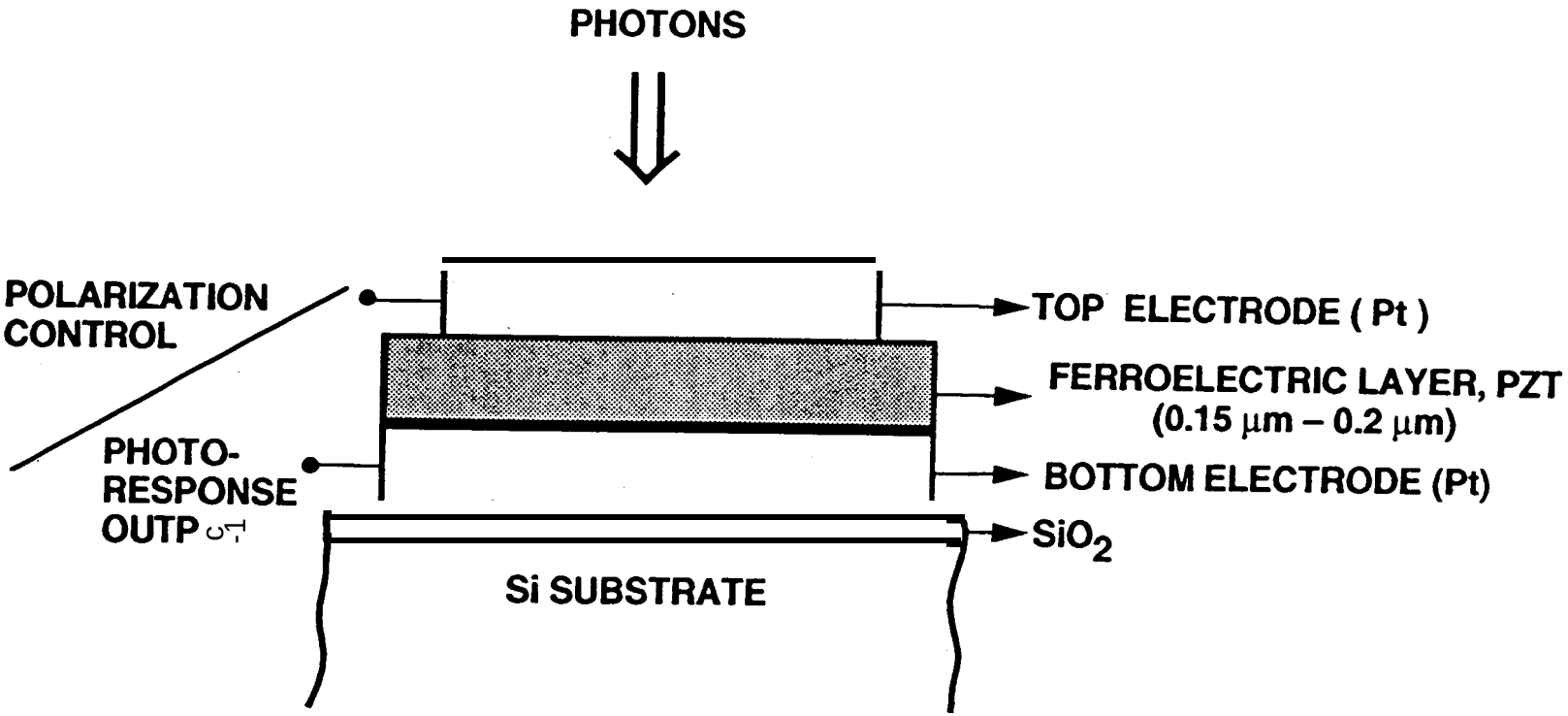

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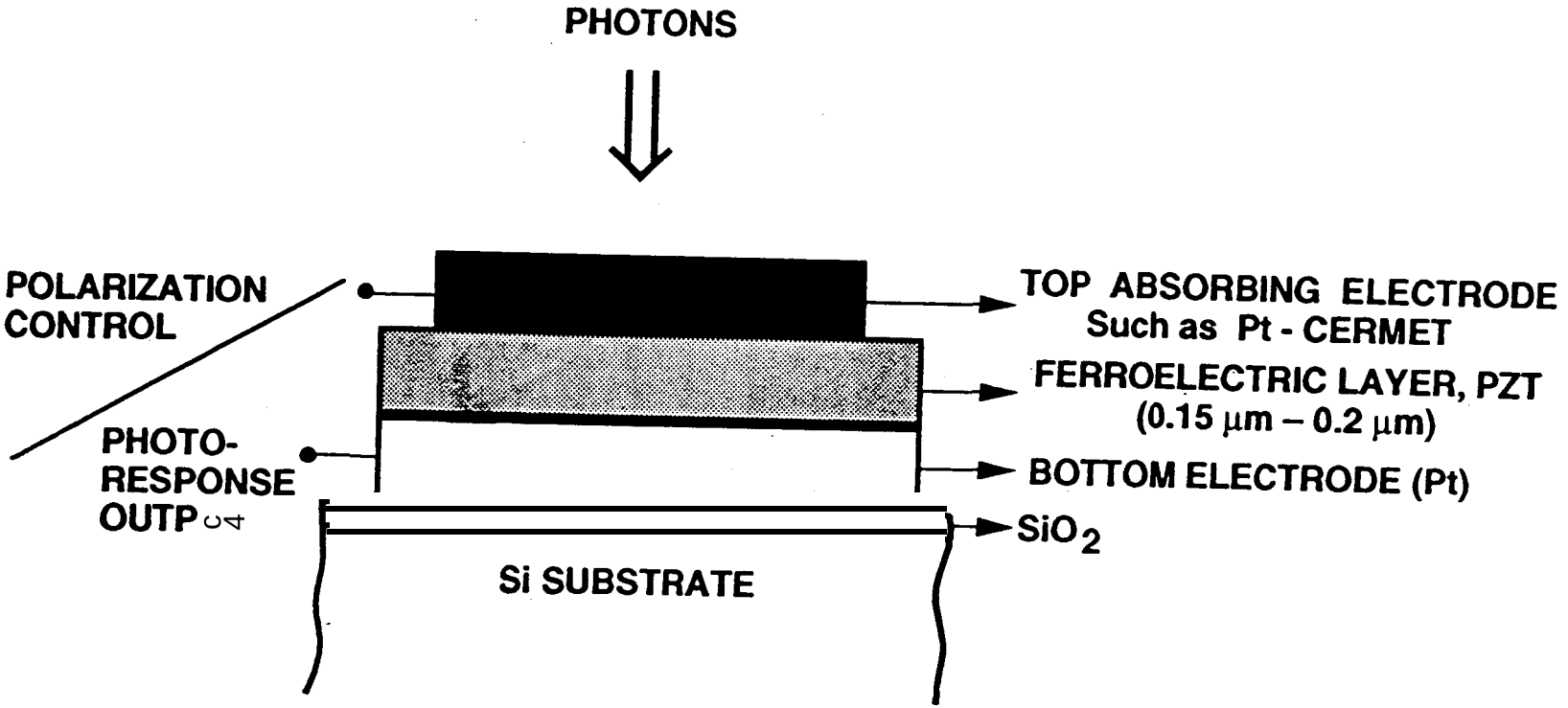
Figure 1(a) of 6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TOP ABSORBING ELECTRODE
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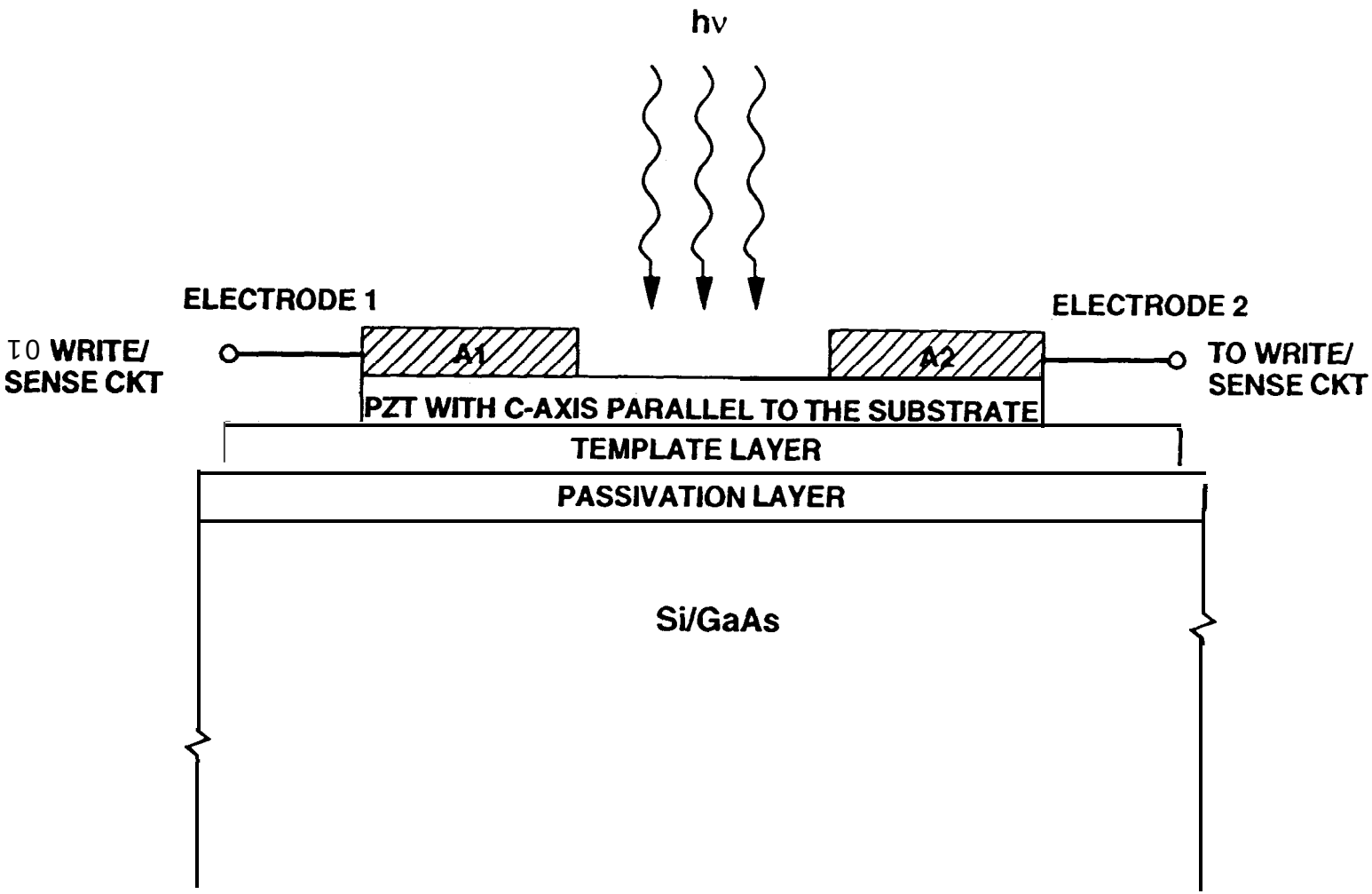

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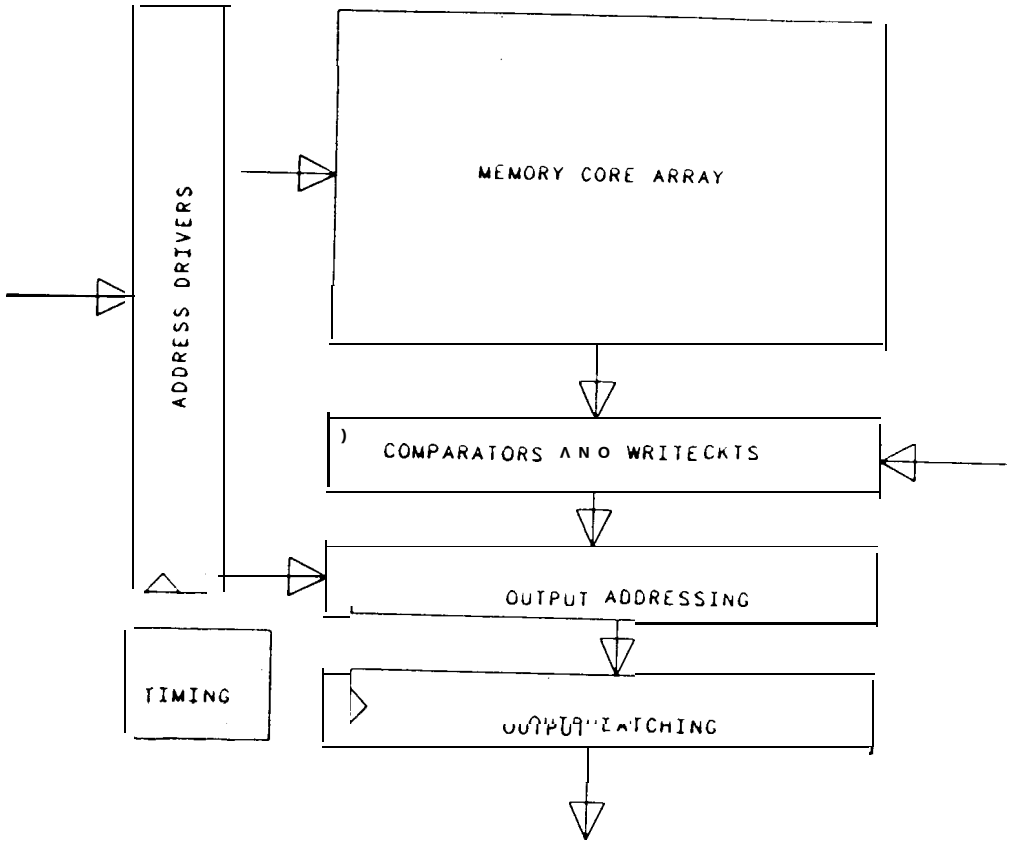
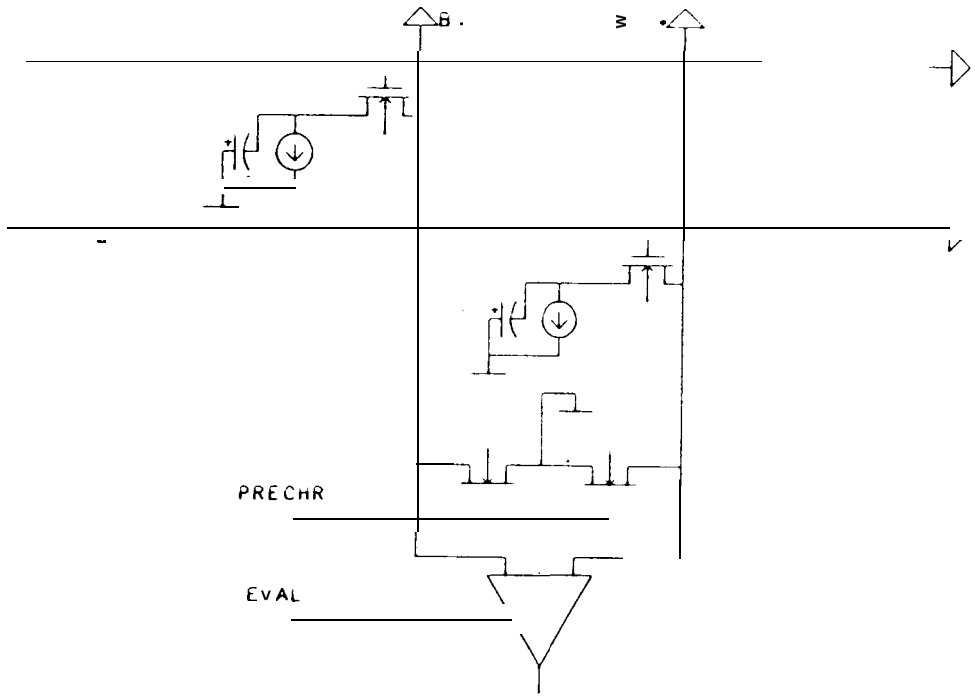
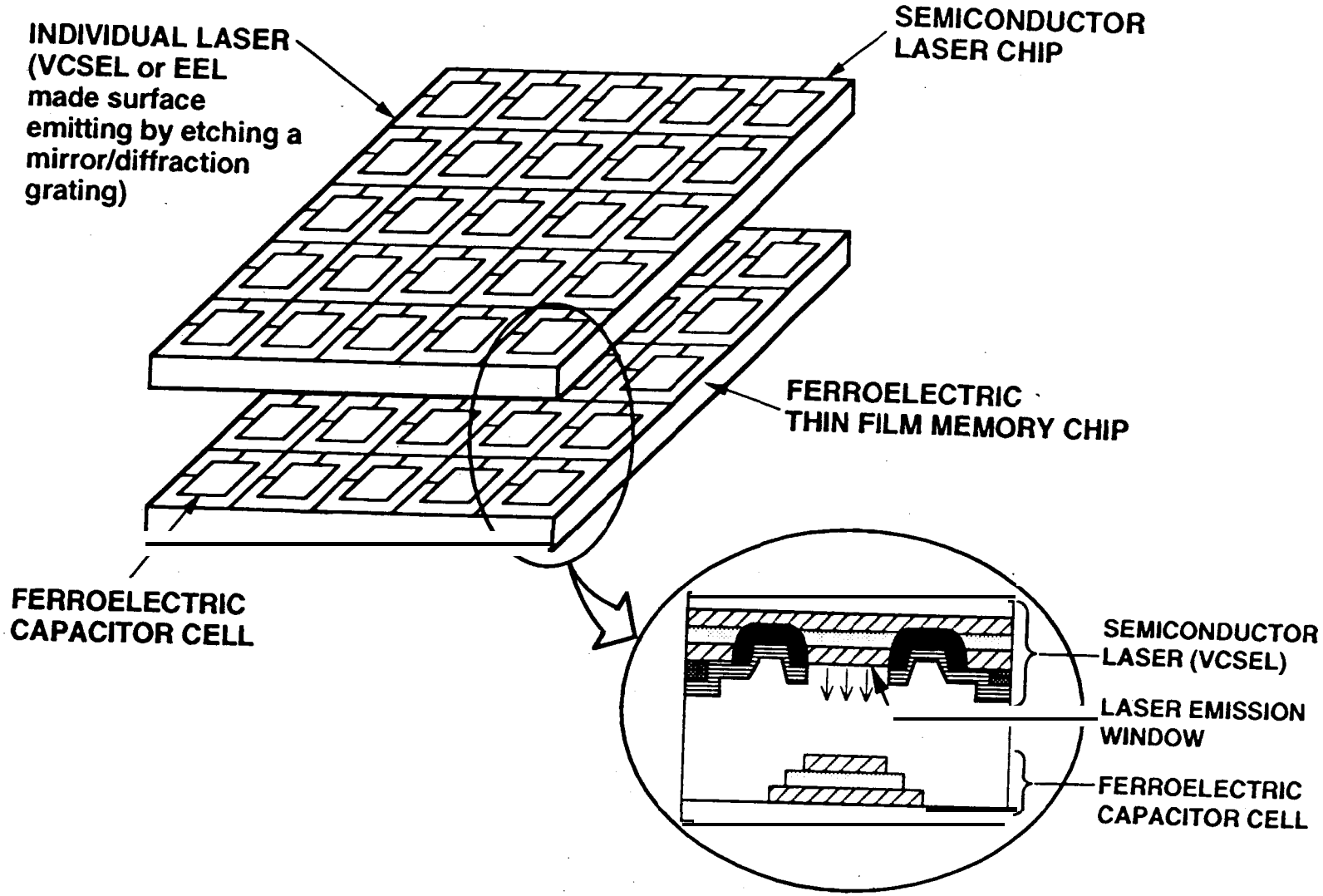

ADDRESS DRIVERS
MEMORY CORE ARRAY
COMPARATORS AND WRITECKTS
OUTPUT ADDRESSING
TIMING



0 DEMUX AND LATCH



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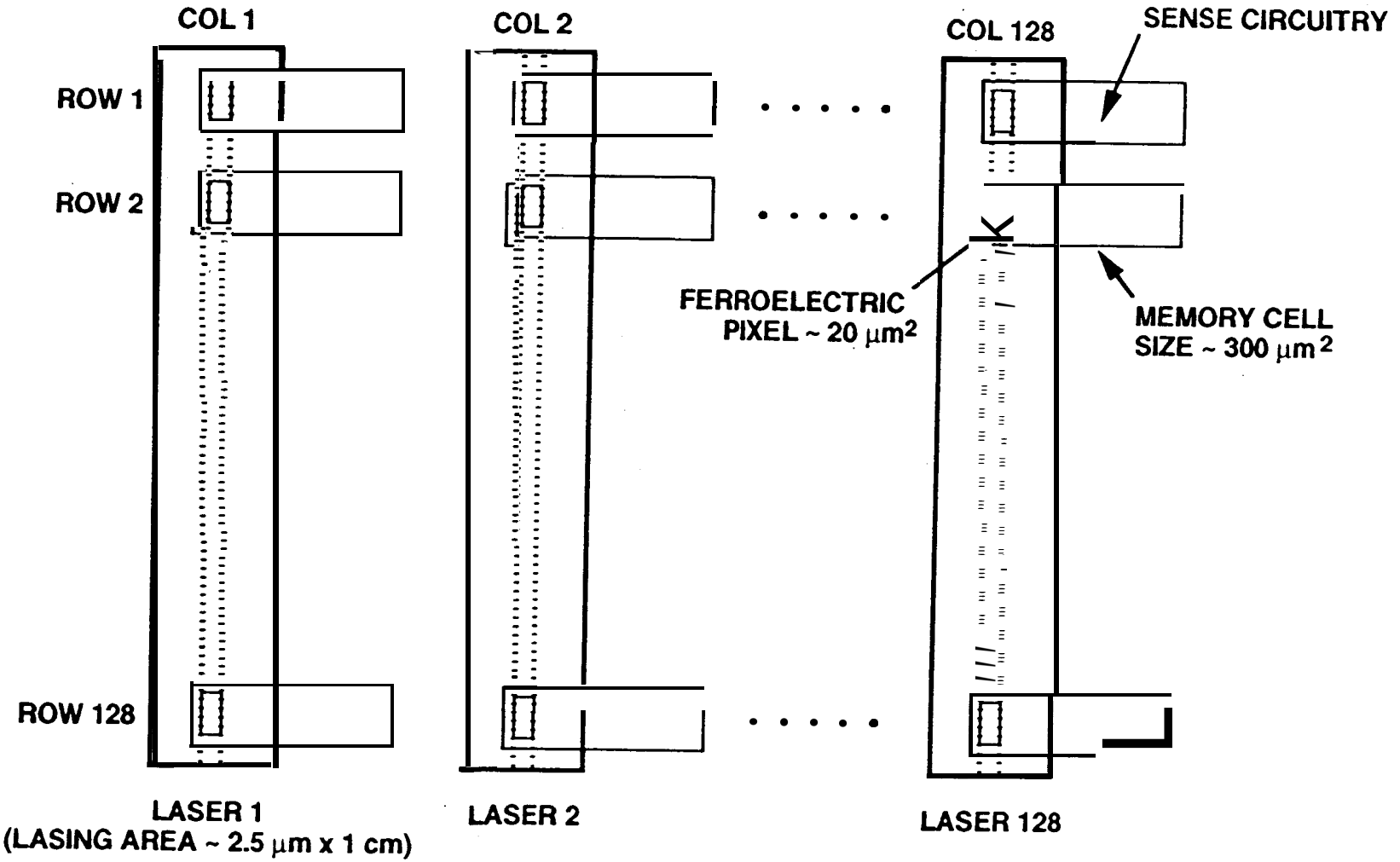
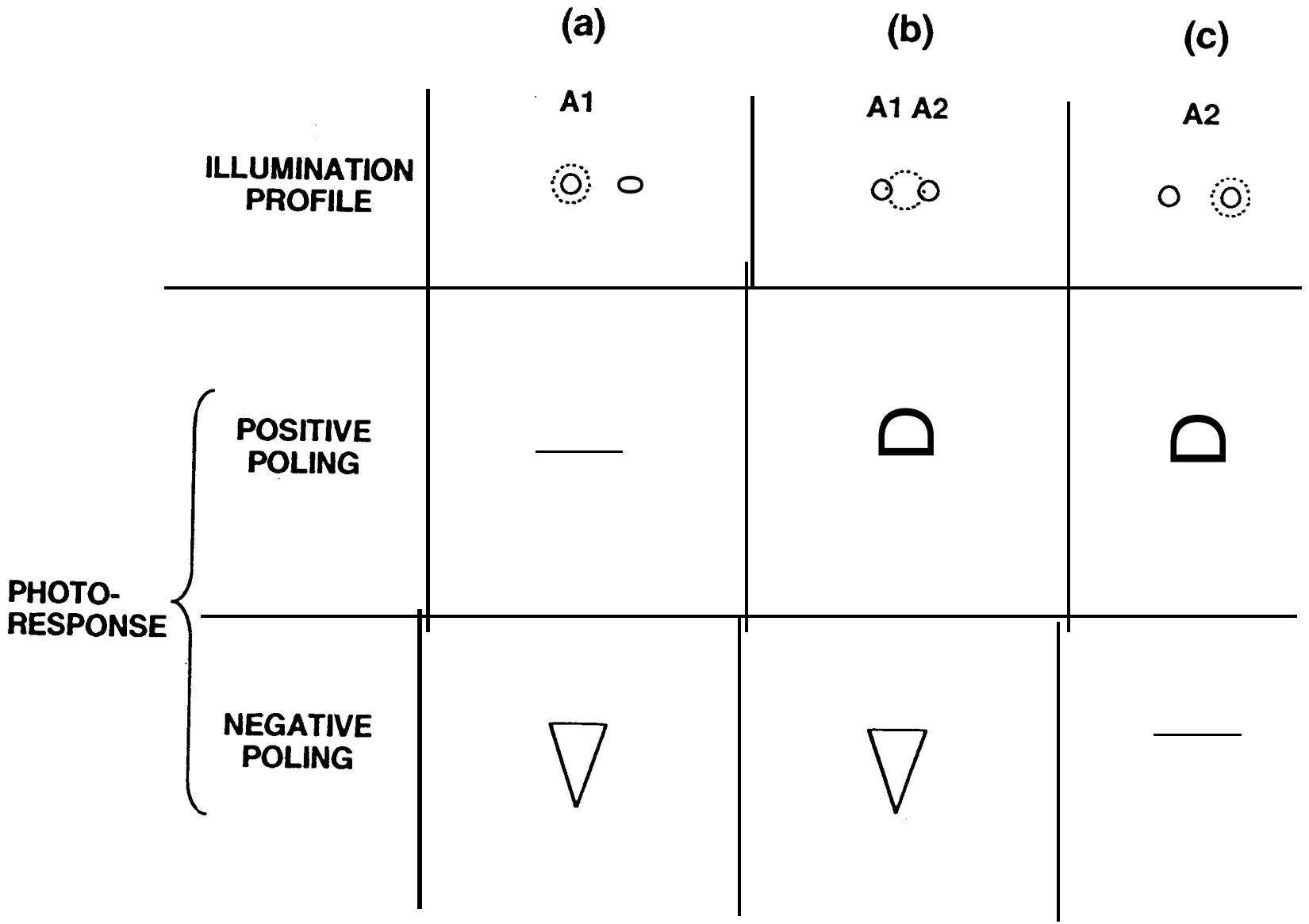

COL 1
COL 2
COL 128
SENSE CIRCUITRY
ROW 1
ROW 2
ROW 128
FERROELECTRIC
PIXEL ~ 20 μm²
MEMORY CELL
SIZE ~ 300 μm²
LASER 1
(LASING AREA ~ 2.5 μm x 1 cm)
LASER 2
LASER 128


(a)
(b)
(c)
A1
A1 A2
A2
ILLUMINATION PROFILE
POSITIVE POLING
NEGATIVE POLING
PHOTO-RESPONSE

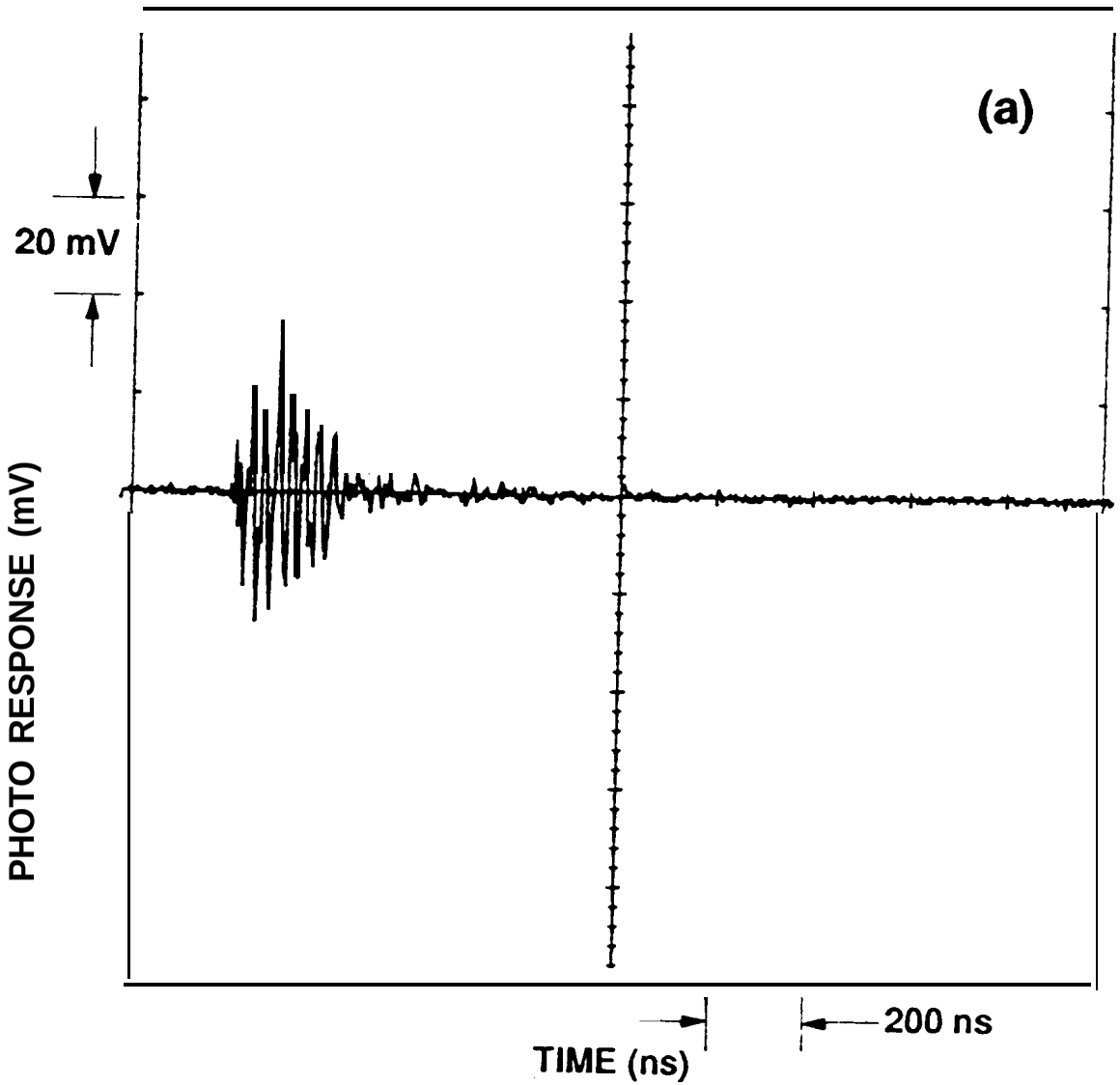


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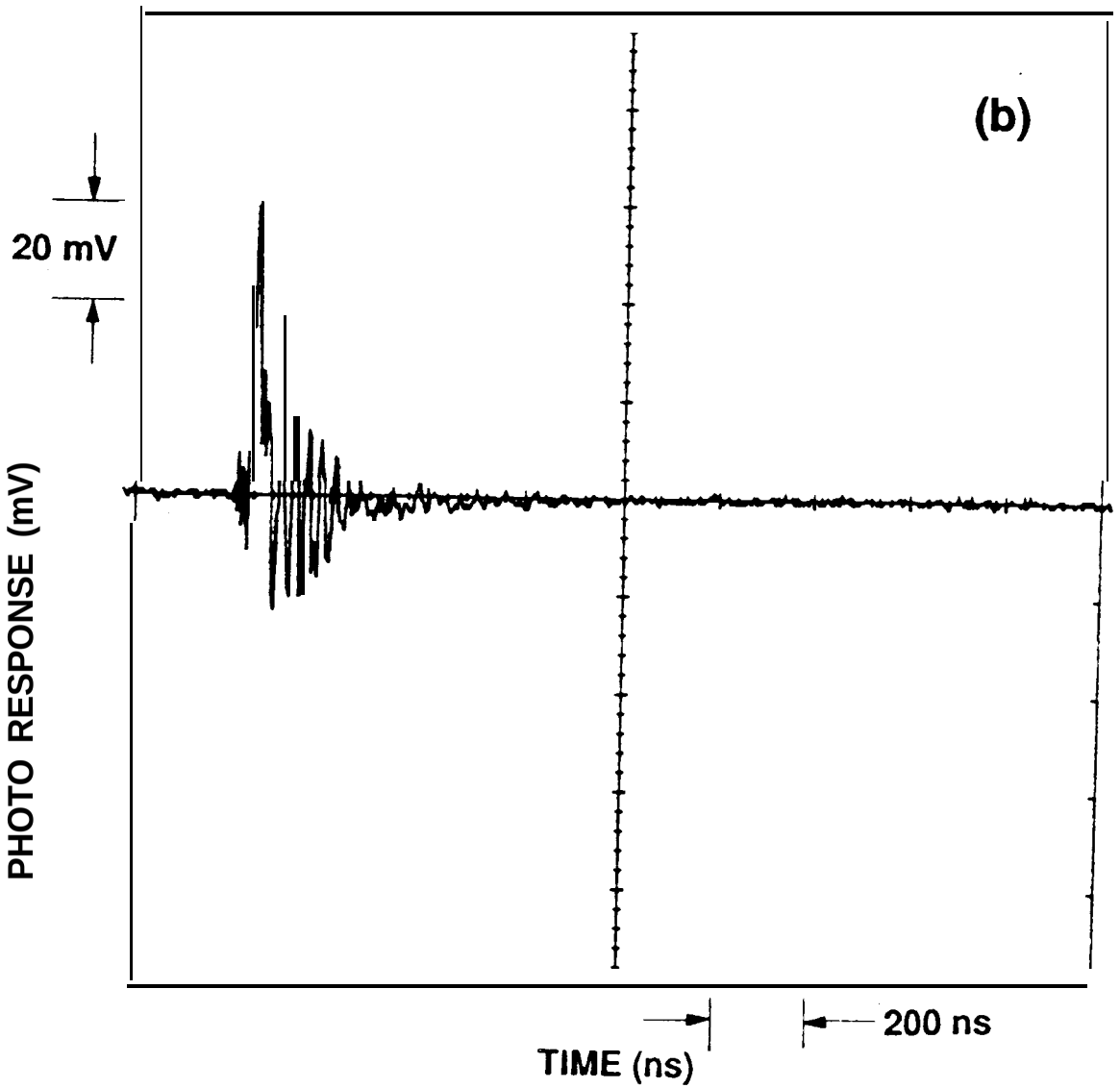
Figure 6(a) of 6


(b)
20 mV
PHOTO RESPONSE (mV)
200 ns
TIME (ns)

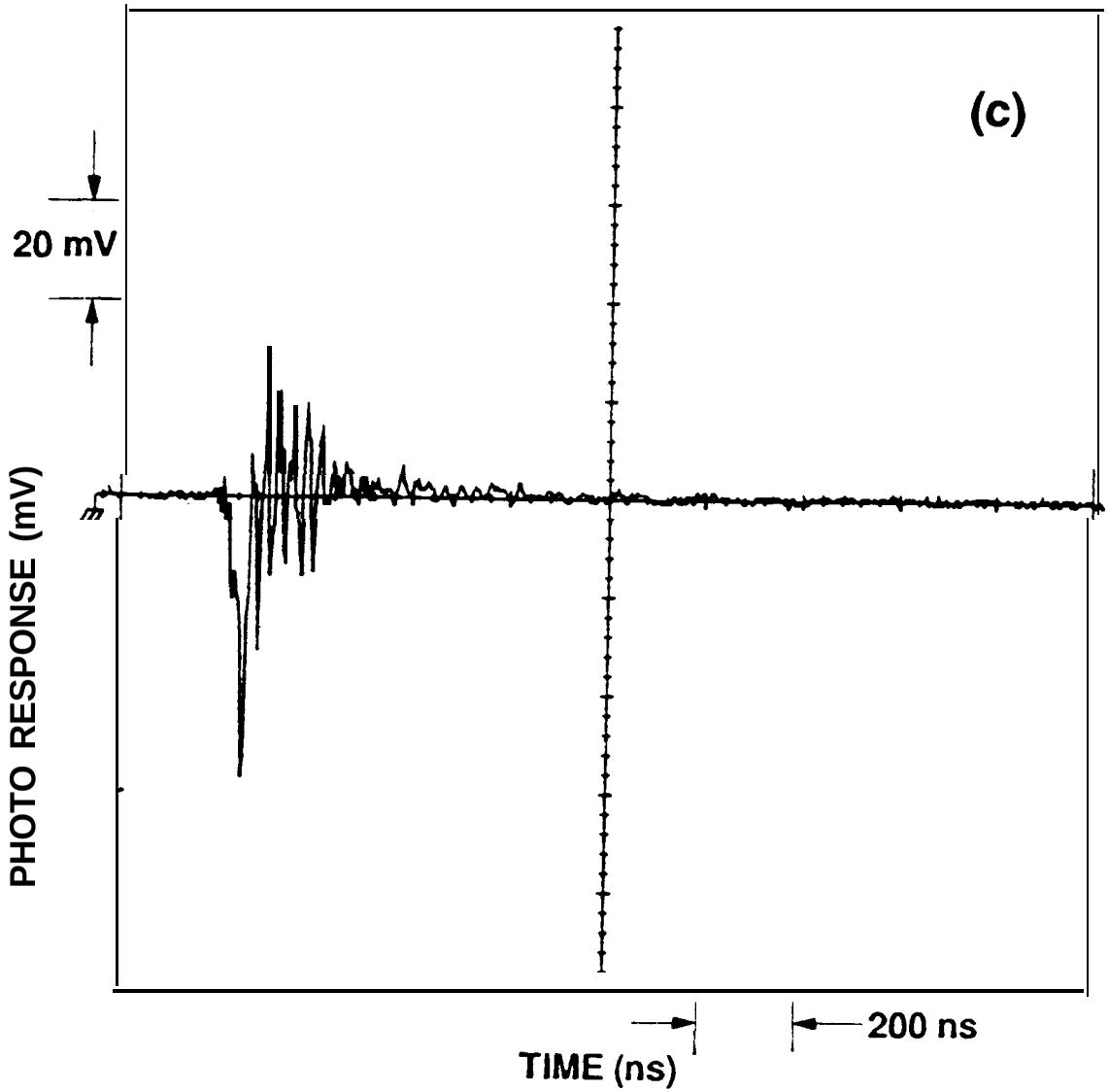


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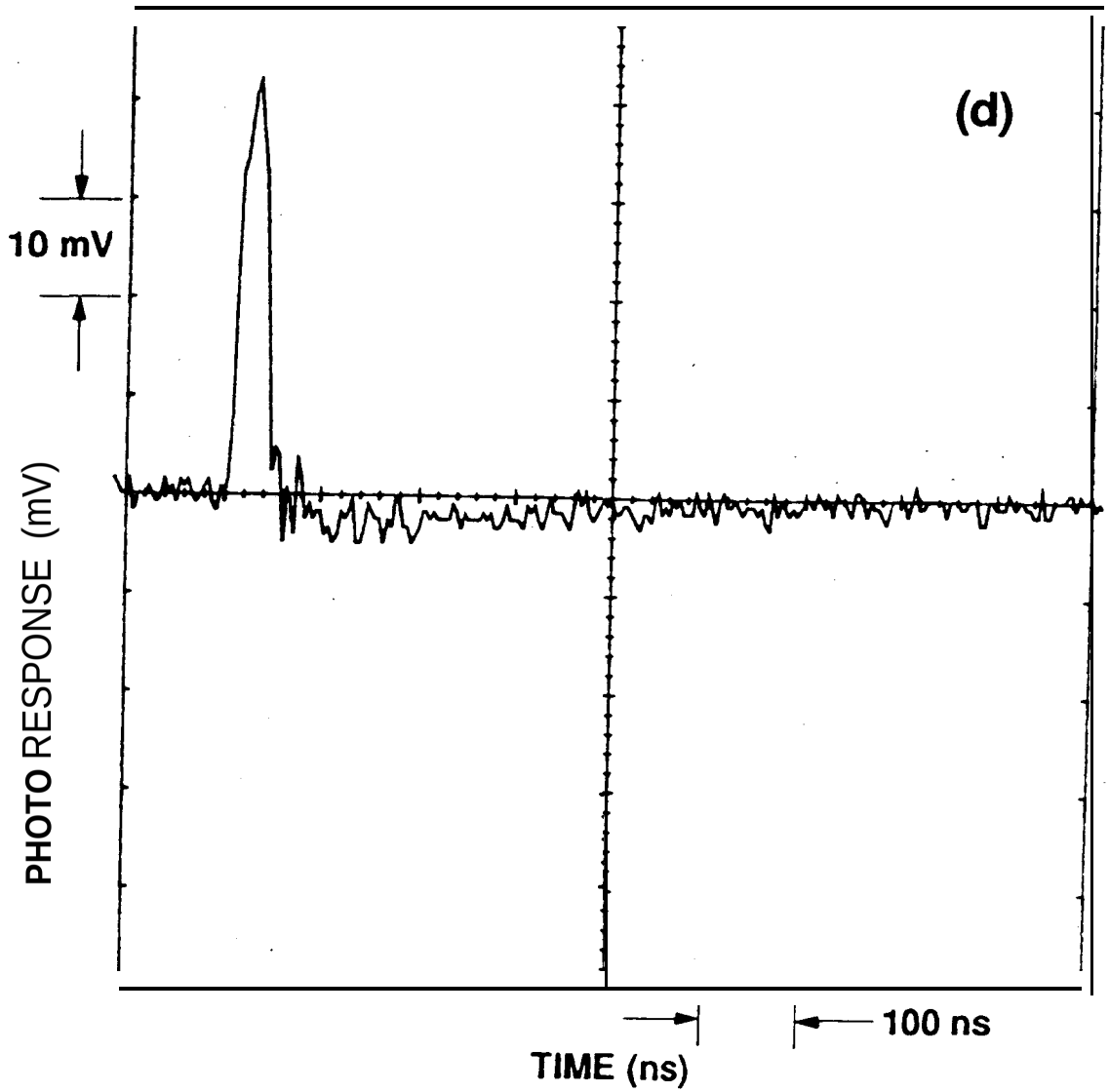
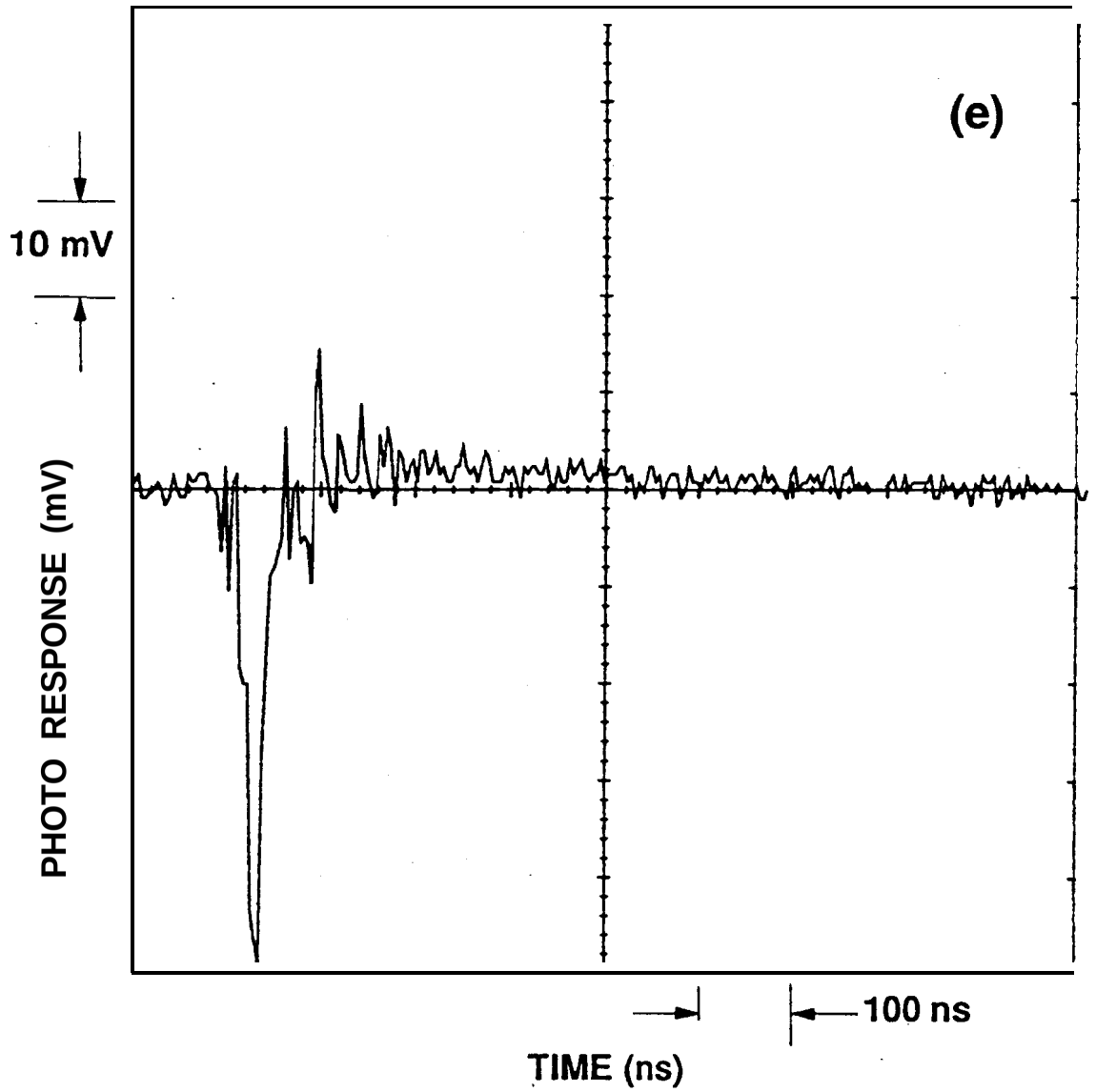
Figure 6(c) of 6


(d)
10 mV
PHOTO RESPONSE (mV)
100 ns
TIME (ns)



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